Current Listing of Claims

Kindly replace any previous listing of claims with the present listing of claims.

1. (currently amended) A digital signal processor comprising:

an instruction memory , a central arithmetic unit, a register, a controller, an event control unit and input/output devices;

[[characterized in that]]

the instruction memory is arranged to include operation code including logical operations, time performance constraints and events;

the controller is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit and resume processing when advised by the event control unit; and

the event control unit is arranged to recognize an event that initiates or resumes processing [[by the event control unit]], wherein the event is an input signal or a completion of processing from a previous event [[and to control processing to be carried out as a consequence of the event while fulfilling the time performance constraints, wherein a pulse package held in the event control unit]] the operation code comprises [[includes]] an event operand [[operable]] arranged to identify the input signal or previous event to initiate or resume processing [[by]] of the event control unit and a delay operand comprising those time performance constraints executed by [[that defines a stop condition for]] a counter in the event control unit.

2. (previously presented) A digital signal processor in accordance with claim 1, wherein the event is detected by the event control unit.

3. (previously presented) A digital signal processor in accordance with claim 2, wherein the event control unit is arranged to detect input signals.

4. (previously presented) A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of the event.

5. (previously presented) A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of a previous event.

6. (previously presented) A digital signal processor in accordance with claim 1, wherein the event control unit includes a signal memory arranged to store and extract data under control of the event control unit.

7. (previously presented) A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory.

8. (canceled).

9. (canceled).

10. (previously presented) A digital signal processor in accordance with claim 1, including two or more event control units arranged to work independently from each other.